

APPLICATION FOR UNITED STATES LETTERS PATENT

FOR

**COMBINATION BACK GRIND TAPE AND UNDERFILL FOR
FLIP CHIPS**

INVENTORS:

Yew Wee Cheong
Marvin R. Diaz
Cheong Huat Ng

PREPARED BY:

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
12400 WILSHIRE BOULEVARD, 7TH FLOOR
LOS ANGELES, CALIFORNIA 90025
(408) 720-8300

Attorney Docket No.: 42P17612

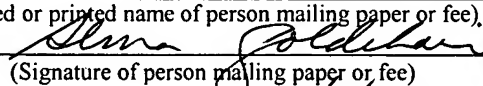
Express Mail Certificate of Mailing

"Express Mail" mailing label number: EV 336581739 US
Date of Deposit: December 11, 2003

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Commissioner for Patents, Mail Stop Patent Application, PO Box 1450, Alexandria, Virginia 22313-1450.

Alma Goldchain

(Typed or printed name of person mailing paper or fee).


(Signature of person mailing paper or fee)

12/11/03
(Date signed)

COMBINATION BACK GRIND TAPE AND UNDERFILL FOR FLIP CHIPS

Inventors:

Yew Wee Cheong
Marvin R. Diaz
Cheong Huat Ng

BACKGROUND

Background of the Invention

[0001] Several semiconductor dice with microelectronic circuitry and devices are fabricated at once on a single wafer. Each die on the wafer may be, for example, a microprocessor. After the circuitry and devices have been fabricated on one side of the wafer, the wafer is thinned by grinding away the side of the wafer opposite the circuitry and devices. To protect the circuitry and devices, back grind tape is applied. After the wafer is thinned, this back grind tape is removed and discarded.

[0002] The wafer is then cut to separate the dice from each other. During this process, a die can be damaged. The singulated dice are connected to substrates by reflow soldering. Underfill material is then applied to the coupled die and substrate assemblies. The underfill material fills space between the die and substrate through capillary action. This underfill is then cured.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Figure 1 is a flow chart that illustrates using a protective layer to protect dice on a wafer during thinning of the wafer and then act as underfill when a chip from that wafer is attached to a substrate.

[0004] Figure 2 is a top view of a fabricated wafer.

[0005] Figure 3a is a cross sectional side view of the wafer illustrating the application of the protective layer according to one embodiment of the present invention.

[0006] Figure 3b is a magnified view of a portion of the cross sectional side view of the wafer of Figure 3a.

[0007] Figure 3c is a cross sectional side view of the wafer illustrating the application of the protective layer according to another embodiment.

[0008] Figure 4 is a cross sectional side view of the wafer and protective layer.

[0009] Figures 5a and 5b are cross sectional side views illustrating the wafer before and after thinning.

[0010] Figure 6a is a cross sectional side view of the wafer with the protective layer being cut to singulate the individual chips.

[0011] Figure 6b is a cross sectional side view that illustrates one die after it has been singulated from the wafer.

[0012] Figure 7 is a cross sectional side view of a die positioned adjacent to and being attached to a substrate while the protective layer is cured.

[0013] Figure 8 is a schematic diagram of a computer system according to one embodiment of the present invention.

DETAILED DESCRIPTION

[0014] Figure 1 is a flow chart 100 that illustrates using a protective layer to protect dice on a wafer during thinning of the wafer according to an embodiment of the present invention. In an embodiment, that protective layer may then act as underfill when a chip from that wafer is attached to a substrate. Note that the flow chart 100 of Figure 1 merely represents one embodiment of the present invention. In other embodiments, some of the steps shown in the flow chart 100 may be omitted, other steps may be added, and/or the steps shown may be performed in a different order.

[0015] After one or more dice are fabricated on a wafer, a protective layer is applied 102 to the wafer. Referring now to Figure 2, a top view of a fabricated wafer 200 is illustrated according to one embodiment of the present invention. During fabrication, a plurality of chips or dice 202 may have been formed on the wafer 200. The words “chip” and “die” are used interchangeably in this document. Each chip or die 202 may comprise microelectronic circuitry or devices. For example, each die 202 may comprise a microprocessor in an embodiment. In other embodiments, the protective layer 102 may be applied to a single chip 202 that is not connected to other chips 202 on a wafer.

[0016] Figure 3a is a cross sectional side view of the wafer 200 taken through reference line 204 of Figure 2, and illustrates the application 102 of the protective layer 302 according to one embodiment. The protective layer 302 may comprise an epoxy film in one embodiment, or may comprise other materials in other embodiments. The protective layer 302 may be applied 102 through mechanical methods, such as by a mechanical roller 306 that may roll a smooth layer of the epoxy film onto the wafer 200. This protective layer 302 may be applied to the top side 304 of the wafer 200, which may

be the side on which the microelectronic circuitry or devices of the chips 202 may be located.

[0017] Figure 3b is a magnified view of a portion of the cross sectional side view of the wafer 200 of Figure 3a that illustrates the wafer 200 after application of the protective layer 302 in more detail. There may be connection structures 308 coupled to the top side 304 of the wafer 200. These connection structures 308 may be solder balls in one embodiment, and may have been applied to the wafer 200 or chip 202 prior to application 102 of the protective layer 302. The protective layer 302 may be thick enough to cover the connection structures 308 extending above the wafer 200 as well as the wafer 200 itself. In one embodiment, the protective layer 302 is at least as high as the connection structures 308 so that the connection structures 308 are completely covered with material of the protective layer 302 after the layer 302 is applied. In an embodiment, the connection structures 308 comprise a eutectic bump with a height of about 3.5 ± 0.9 thousandths of an inch, and the protective layer 302 has a thickness of at least that much. In another embodiment, the connection structures 308 comprise a copper column with a height of about 2 ± 1 thousandths of an inch, and the protective layer 302 has a thickness of at least that much. In other embodiments, the connection structures 308 may comprise other structures with different heights, and the protective layer 302 may have corresponding thicknesses.

[0018] Figure 3c is a cross sectional side view of the wafer 200 taken through reference line 204 of Figure 2, and illustrates the application 102 of the protective layer 302 according to a second embodiment. Figure 3c illustrates the application of the protective layer 302 through use of a vacuum, or pressure differential. A region of

higher pressure 310 may be above the protective layer 302, and a region of lower pressure 312 may be below the protective layer 302. The difference in pressures of these two regions may apply 102 the protective layer 302 by pressing the protective layer 302 into position on the top side 304 of the wafer 200.

[0019] Returning to Figure 1, the protective layer 302 may be partially cured 104 after it is applied 102 to the wafer 200 in one embodiment. Referring now to Figure 4, a cross sectional side view of the wafer 200 and protective layer 302 is illustrated. In an embodiment, the protective layer 302 may comprise epoxy, and heat 400 may be applied to the protective layer 302 to partially cure the epoxy. In other embodiments, the epoxy may be partially cured with a different method. In yet other embodiments, the protective layer 302 may comprise other materials than epoxy and the protective layer 302 may be partially hardened with a process appropriate to the material used rather than partially cured. This partial curing 104, or other partial hardening process, may help the protective layer 302 to adhere to the wafer 200 during subsequent processing, and add structural rigidity to better protect the wafer 200 and any microelectronic circuits or devices on the chips 202 of the wafer 202 during subsequent processing.

[0020] Returning to Figure 1, the wafer 200 may then be thinned 106. Referring now to Figure 5a, a cross sectional side view of the wafer 200 and protective layer 302 is illustrated. The wafer 200 shown in Figure 5a has been flipped upside down so that the top 304 side of the wafer 200 is toward the bottom of Figure 5a, and the bottom side 502 of the wafer 200 is toward the top of Figure 5a. The wafer 200 may have an initial thickness 504 after the microelectronic circuits or devices on the chips 202 of the wafer 200 have been fabricated. In an embodiment, the original thickness 504 may be in a

range from 28 to 32 thousandths of an inch thick. In other embodiments, the wafer 200 may have a different initial thickness 504. Some of the material from the bottom 502 of the wafer 200 may be removed to reduce the thickness of the wafer 200 and result in a smaller thickness 506, as shown in Figure 5b. In an embodiment, this smaller thickness 506 may be in a range of about 2 to 17 thousandths of an inch less than the initial thickness 504. In other embodiments, varying smaller thicknesses 506 may result from the thinning process. This smaller thickness 506 may be achieved by grinding away some of the material on the bottom 502 of the wafer 200. During such grinding, the protective layer 302 may protect from damage the top 304 of the wafer 200, any microelectronic circuits or devices on the chips 202 of the wafer 200, and the connection structures 308 connected to the top 304 of the wafer.

[0021] Returning to Figure 1, the wafer 200 may be mounted 108 on a frame, which may hold the wafer 200 in position while the wafer 200 is cut to separate 110 the individual chips 202 from the wafer 200 and each other. Referring now to Figure 6a, a cross sectional side view of the wafer 200 with the protective layer 302 mounted in a frame 602 and being cut to separate 110 the individual chips 202 from the wafer 200 and each other, also known as singulating the chips 202, is illustrated. A rotating saw blade 604 may be used to cut apart the wafer 200 into multiple chips 202 in one embodiment. During this cutting, the protective layer 302 may protect the chips 202, and any microelectronic circuits or devices on the chips 202, from being damaged during the cutting process, or from particulate matter created during the cutting process that could otherwise contaminate the microelectronic circuits or devices on the chips 202.

[0022] Figure 6b is a cross sectional side view that illustrates one die 202 after it has been singulated from the wafer 200, according to one embodiment of the present invention. As illustrated, the bottom side 502 of the die 202 is toward the top of Figure 6b, and the top 304 of the die 202, which may have microelectronic circuits or devices, is toward the bottom of Figure 6b. A portion of the protective layer 302 that covers the die 202 has also been cut during the singulation process, so remains covering the die 202. The term “protective layer 302” may refer to both the layer 302 that covers the entire wafer 200 and the portion 302 of the layer that covers a single die 202 after singulation. The protective layer 302 may also cover connection structures 308 that are coupled to the die 302 in an embodiment. In one embodiment, the protective layer 302 may substantially cover the connection structures 308, but not extend substantially further from the top 304 of the die 202 than the point of the connection structures 308 that is farthest from the die 202. In another embodiment, the protection layer 302 may have a thickness larger than the height of the connection structures 308 so that the protection layer 302 extends farther from the top 304 of the die than the connection structures 308 do.

[0023] Returning to Figure 1, the chip 202 may be positioned 112 on a substrate to which that chip 202 may be attached. The chip 202 may then be attached 114 or connected 114 to the substrate. The protective layer 302 may also be fully cured 114. Referring now to Figure 7, a cross sectional side view of a die 202 positioned 112 adjacent to a substrate 702 and being attached 114 to the substrate 702 while the protective layer 302 is cured 114 according to one embodiment of the present invention, is illustrated. When positioning 112 the die 202 on the substrate 702, the connection

structures 308 may be positioned so that they may both electrically and structurally connect the die 202 to the substrate 702. In an embodiment, since the protective layer 302 may have been only partially cured, the protective layer 302 may maintain some flexibility. This may allow the connection structures 308 to force any material of the protective layer 302 between the edge of the connection structure 308 and the substrate 702 out of the way while the die 202 is pressed to the substrate 702, to allow the connection structure 308 to contact the substrate 702 even if the protective layer 302 had extended beyond the connection structure 308 prior to positioning 112 the die 202 adjacent the substrate 702.

[0024] Heat 704 may be applied to the top or bottom of the die 202/substrate 702 assembly. In an embodiment where the connection structures 308 comprise solder, this heat 704 may cause some of the solder to melt, to reflow solder connect the die 202 to the substrate 702. This reflow soldering may thus attach 114 the die 202 to the substrate 702. In an embodiment where the protective layer 302 comprises epoxy, such as a heat curable epoxy, the heat 704 may also fully cure 114 the protective layer 302, which may then act as underfill between the die 202 and substrate 702. Thus, a portion of the protective layer 302 applied 102 to the wafer 200 may remain between the die 202 and substrate 702 after the die 202 has been singulated from the wafer 200 and attached to the substrate 702.

[0025] Figure 8 is a schematic diagram of a computer system 802 according to one embodiment of the present invention. The computer system 802 may include the die 202 attached to the substrate 702, with the protective layer 302 between the die 202 and substrate 702, as described above. The substrate 702 may be connected to a structure

such as a printed circuit board ("PCB") 808 by connectors such as solder balls 810 or other connectors. Additionally, the computer system 802 may include a memory 812 and/or a mass storage unit 814, and/or other components which may be connected to the PCB 808. The memory 804 may be any memory, such as random access memory, read only memory, or other memories. The mass storage unit 814 may be a hard disk drive or other mass storage device. The computer system 802 may also include other components such as input/output units, a microprocessor, or other components.

[0026] The foregoing description of the embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. This description and the claims following include terms, such as left, right, top, bottom, over, under, upper, lower, first, second, etc. that are used for descriptive purposes only and are not to be construed as limiting. The embodiments of a device or article described herein can be manufactured, used, or shipped in a number of positions and orientations. Persons skilled in the relevant art can appreciate that many modifications and variations are possible in light of the above teaching. Persons skilled in the art will recognize various equivalent combinations and substitutions for various components shown in the Figures. It is therefore intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.